an access device;

a memory element operatively coupled to the access device, the memory element comprising:

dielectric material having a pore therein, the pore being smaller than a photolithographic limit;

a first electrode disposed within the pore;

a memory material disposed over the first electrode; and

a second electrode disposed over to the memory material; and

wherein at least one of the access device and the memory element is disposed wholly in the area.

47 (once amended). A memory cell comprising:

an area defined by an intersection of a word line and a bit line;

an access device;

a memory element operatively coupled to the access device, the memory element comprising a memory material disposed between a first electrode and a second electrode; and

dielectric material having a pore therein, the pore being smaller than a photolithographic limit, wherein at least one of the first electrode, the memory material, and the second electrode is disposed within the pore; and

wherein at least one of the access device and the memory element is disposed wholly in the area.

Please add new claims 77-91 as set forth below:

77 (new). An X-point memory cell comprising:

a first conductive line extending in a first direction;

a second conductive line extending in a second direction different than the first direction, the first conductive line and the second conductive line being spaced apart by a portion of a substrate, the second conductive line intersecting the first conductive line in an overlapping manner to form an area of intersection in the portion of the substrate;

an access device wholly disposed in the area of intersection, the access device being operatively coupled to one of the first conductive line and the second conductive line; and

a memory element wholly disposed in the area of intersection, the memory element being operatively coupled to the access device, the memory element comprising a memory material disposed between a first electrode and a second electrode.

78 (new). The memory cell, as set forth in claim 77, wherein the access device comprises a diode.

79 (new). The memory cell, as set forth in claim 78, wherein the diode comprises:

a layer of N doped polysilicon disposed adjacent a layer of P doped polysilicon.

80 (new). The memory cell, as set forth in claim 77, wherein the first electrode is comprised of a plurality of layers.

81 (new). The memory cell, as set forth in claim 77, wherein the first electrode is comprised of a plurality of materials.

82 (new). The memory cell, as set forth in claim 77, wherein the first electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

83 (new). The memory cell, as set forth in claim 77, wherein the second electrode is comprised of a plurality of layers.

84 (new). The memory cell, as set forth in claim 77, wherein the second electrode is comprised of a plurality of materials.

85 (new). The memory cell, as set forth in claim 77, wherein the second electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

86 (new). The memory cell, as set forth in claim 77, wherein the memory material comprises structure changing material.

87 (new). The memory cell, as set forth in claim 86, wherein the structure changing material comprises a material which changes between different states of crystallinity in response to electrical stimulus.

88 (new). The memory cell, as set forth in claim 87, wherein each of the different states of crystallinity corresponds to a given resistance level.

89 (new). The memory cell, as set forth in claim 77, wherein the memory material comprises a chalcogenide material.